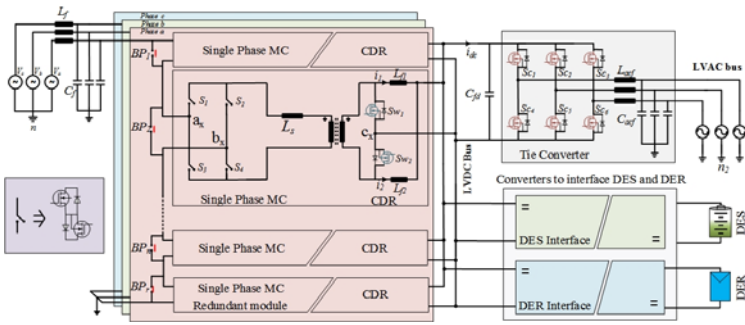


Matrix-Based Solid-State-Transformer (SST) for a Hybrid-Nanogrid

Jaydeep Saha, Gorla Naga Brahmendra Yadav, Sanjib Kumar Panda

Topology

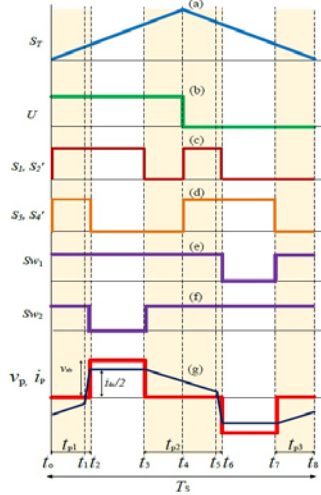
- Facilitates controlled energy-interactions with the grid and the hybrid AC/DC Nanogrid.
- Modular → Grid-side Series, Hybrid-Nanogrid side Parallel.
- Front-end Matrix Converter followed by Current-Doubler-Rectifier (CDR) to form the stiff DC bus.
- 'Tie-Converter' interfaces the Nanogrid's AC and DC distribution networks.



Topology of the Front-end Matrix-based SST

Modes of Operation

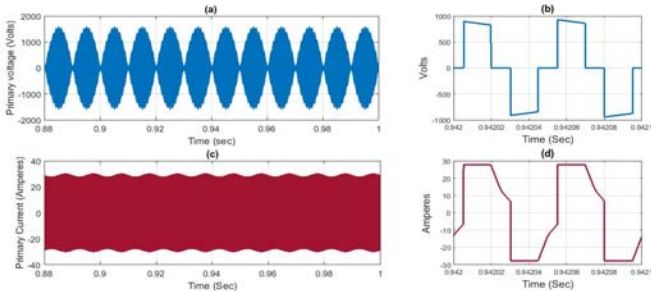
- DC-AC/AC-DC part is critically analysed.
- Modulation index, m_{HF} for Matrix-Converter:



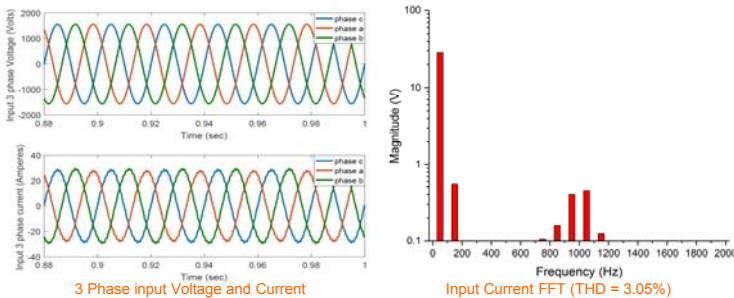
- Modulation index, m_a for Tie-Converter:

(a) Triangular Carrier Wave
 (b) Inversion signal (c) Switching pulse for the top pair of switches in MC (d) Switching pulse for the bottom pair of switches in MC (e) Switching Pulse for the CDR bottom-switch Sw1 (f) Switching Pulse for the CDR top-switch Sw2 (g) High-frequency Voltage and current waveform in the primary-side of the Transformer

Simulation Results

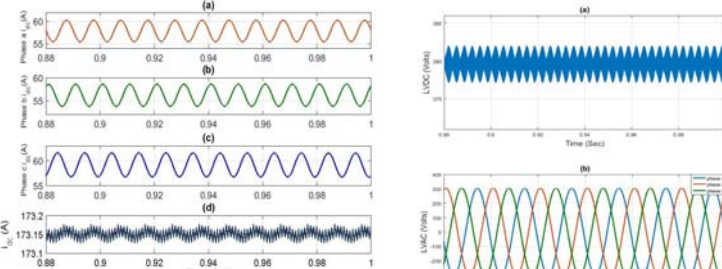


(a) HVAC voltage at the primary of HF transformer (b) Magnified view of the HFAC voltage (c) HFAC current at the primary of HF transformer (d) Magnified view of the HFAC current



3 Phase input Voltage and Current

Input Current FFT (THD = 3.05%)



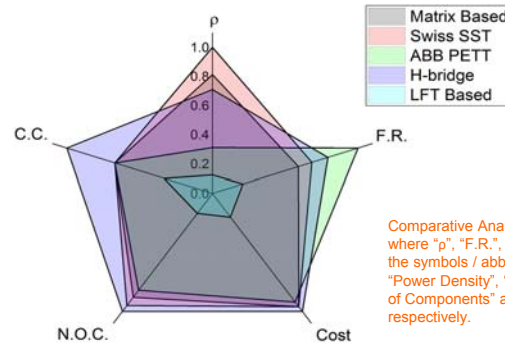
DC rippled currents (a) emerging from phase 'a' CDR (b) emerging from phase 'b' CDR (c) emerging from phase 'c' CDR (d) i_{dc}

(a) LVDC voltage (b) LVAC voltage

- The currents emerging from CDRs in each phase (having ~5A ripple) meet to produce a lower current ripple (~0.06A).
- LVDC bus voltage has ~2% voltage ripple and LVAC bus voltage has minimum distortions.

Comparative Analysis

Criteria \ Topology	Matrix-Based SST	Swiss SST	ABB's PETT	Cascaded H-bridge	STATCOM based LFT
Power Density (kW/L)	1.95	2.4 [12]	0.75 [3]	1.7 [10]	0.3 [11]
Failure Rate (hr ⁻¹)	1.963*10 ⁻⁴	2.28*10 ⁻⁴	3.34*10 ⁻⁴	2.65*10 ⁻⁴	0.7*10 ⁻⁴
Cost (USD/kW)	54	54	51.6	56.2	11.4 [11]
No. of Components	58	63	54	66	11
Control Complexity	2	2	2	3	1



Comparative Analysis of SST topologies, where "p", "F.R.", "N.O.C." and "C.C." are the symbols / abbreviations assigned to "Power Density", "Failure Rate", "Number of Components" and "Control Complexity" respectively.

- Random failure-rate of Aluminum Electrolytic Capacitors:

$$\lambda_C = \frac{4 * 10^6 * N * V_a^3 * C^{0.5} * 2^{(T_a - T_m)}}{L_b * V_r^2}$$

- Reliability of the proposed topology is superior among the SSTs.
- Line-frequency transformer's power density is quite low compared to any SST.

Conclusions

- Single-stage DC-AC/AC-DC conversion.
- Eliminates one electrolytic capacitor due to direct Line-frequency AC to High-frequency AC conversion by Matrix-Converters.
- Current-ripple cancellation after CDR stage leads to reduction of the stiff-DC link capacitor size.
- A theoretical increment in reliability.
- Quite high power-density can be achieved.
- Grid-side current harmonic content is quite low – this is attributed to the Modulation scheme of the Matrix-Converter.

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